UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,886	07/30/2003	Arthur R. Alexander	11279 (NCR.0111US)	7940

26890 7590 03/31/2009

JAMES M. STOVER
TERADATA CORPORATION
2835 MIAMI VILLAGE DRIVE
MIAMISBURG, OH 45342

EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

MAIL DATE	DELIVERY MODE
03/31/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ARTHUR R. ALEXANDER, JUN FAN,
JAMES L. KNIGHTEN, and NORMAN W. SMITH

Appeal 2009-1307
Application 10/630,886
Technology Center 2800

Decided:[1] March 31, 2009

Before JOSEPH F. RUGGIERO, MARC S. HOFF,
and CARLA M. KRIVAK, *Administrative Patent Judges*.

KRIVAK, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134 from a final rejection of claims 15 and 25. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

---

[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF CASE

Appellants' claimed invention is a circuit board that includes resistive elements and/or buried decoupling capacitors between reference plane layers (¶ [09]). The circuit board package includes any package that has multiple layers of signal wires or conductors and power or ground reference planes (¶ [020]; Fig. 1).

Independent claim 15, reproduced below, is representative of the subject matter on appeal.

> 15. A circuit board comprising:
> a first reference plane layer;
>
> a second reference plane layer;
>
> a dielectric layer between the first and second reference plane layers;
>
> a decoupling capacitor having first and second electrodes; and
>
> a discrete resistor having first and second electrodes, the resistor's first electrode electrically connected to the first reference plane layer, the resistor's second electrode electrically connected to the decoupling capacitor's first electrodes, and the decoupling capacitor's second electrode electrically connected to the second reference plane layers.

REFERENCES

Sunahara	US 6,153,290	Nov. 28, 2000
Chakravorty	US 6,611,419 B1	Aug. 26, 2003

The Examiner rejected claim 15 under 35 U.S.C. § 102(b) based upon the teachings of Sunahara.

The Examiner rejected claim 25 under 35 U.S.C. § 103(a) based upon the teachings of Sunahara and Chakravorty.

Appellants contend that Sunahara does not teach or suggest the reference plane layers recited in the claims (App. Br. 4)

ISSUE

Did the Examiner establish that the wiring conductors of Sunahara are the same as the reference plane layers of Appellants' claimed invention?

FINDINGS OF FACT

1. Appellants' claimed invention discloses signal layers 102, 106, 114, and 118 (Fig. 1) for carrying signal wires and reference plane layers 104, 108, 112, and 116 (Fig. 1). The reference plane layers can contain either a ground plane or a power supply voltage plane connected to a power supply voltage (¶ [021].

2. Sunahara teaches a multilayer ceramic substrate including a plurality of laminated ceramic layers formed of a ceramic insulating material and a wiring conductor. A passive component is built into the laminate and is wired through the wiring conductor (col. 3, ll. 34-39). A series of via-holes are disposed in advance on the ceramic layers for forming the wiring conductors (col. 6, ll. 60-63).

PRINCIPLES OF LAW

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior

art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of Calif., Inc.*, 814 F.2d 628, 631 (Fed. Cir. 1987).

The Examiner bears the initial burden of presenting a prima facie case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). If that burden is met, then the burden shifts to the Appellants to overcome the prima facie case with argument and/or evidence. *See Id.*

ANALYSIS

Anticipation of Claim 15

The Examiner rejected claim 15 under 35 U.S.C. § 102(b) as anticipated by Sunahara. The Examiner finds that the wiring conductor layer of Sunahara is "formed as a layer on a planar surface or a surface plane of the ceramic layers (2, 3 and 7, 8)" (Ans. 5). Thus, the wiring conductor is a wiring conductor plane layer (Ans. 6). The Examiner further asserts that Appellants did not show specific dimensions or size of the plane layers (Ans. 6).

Appellants contend the wiring conductors in Sunahara are not equivalent to the claimed reference plane layer (App. Br. 4). Appellants assert that Sunahara's wiring conductors are formed by providing a laminate with wiring conductors for completing wiring among a capacitor, inductor, resistor, and outer terminal conductors (App. Br. 4). This is contrary to the claimed reference plane layer as Appellants' Specification teaches both signal layers for carrying signal wires or conductors *and* power or ground reference plane layers (emphasis added) (FF 1; App. Br. 4). Sunahara's wiring conductors are clearly signal wires or conductors. This interpretation of the wiring conductors is supported by Sunahara's description that a series

of via-holes are disposed in advance on the ceramic layers for forming the wiring conductors (FF 2) and by the fact that there are two individual wiring conductors (16, 17) shown on the same plane/layer in Fig. 1. Therefore, Sunahara's wiring conductors are just that, wires and not planes, and do not to correspond to the Appellants' claimed reference plane layers.

In view of the above, it is apparent that the Examiner misinterpreted the meaning of "wiring conductors" in Sunahara. Further, the Examiner did not provide evidence or reasoning why a wiring conductor corresponds to a reference plane layer. The Examiner merely stated it is so, and alleged that Appellants did not provide specific dimensions or sizes of the reference plane layer. However, requiring specific dimensions or sizes is not necessary.

Therefore, since not every element as set forth in claim 15 is found, either expressly or inherently, in Sunahara, Sunahara does not anticipate claim 15, and the rejection of claim 15 under 35 U.S.C. § 102 is not sustained.

Obviousness of Claim 25

The Examiner rejected claim 25 as obvious under 35 U.S.C. § 103 over Sunahara and Chakravorty. The Examiner finds that Sunahara teaches all the limitations of claim 25 except for the circuit board having an IC device mounted thereon (Ans. 4).

Appellants contend that because Sunahara does not teach the reference plane layer, then adding an IC device thereon, such as taught by Chakravorty, would not result in Appellants' claimed invention. That is, neither Sunahara nor Chakravorty teach or suggest "'a discrete resistor

having first and second electrodes, the discrete resistor's first electrode electrically connected to the first reference layer'" (App. Br. 5).

Because Sunahara does not teach or suggest reference plane layers as found above, combining Sunahara and Chakravorty would not result in Appellants' claimed invention. Therefore, the rejection of claim 25 under 35 U.S.C. § 103 is not sustained.

CONCLUSION

The Examiner has not provided a prima facie case of obviousness showing that wiring conductors are the same as reference plane layers and thus erred in rejecting claim 15 under 35 U.S.C. § 102 and claim 25 under 35 U.S.C. § 103.

DECISION

The Examiner's decision rejecting claims 15 and 25 is reversed.

REVERSED

KIS

JAMES M. STOVER
TERADATA CORPORATION
2835 MIAMI VILLAGE DRIVE
MIAMISBURG OH 45342